CLAIMS

1. A method comprising:

selecting one of a plurality of debugging modes as a function of a current operating mode of a processor.

2. The method of claim 1 further comprising raising an exception after executing an instruction.

3. The method of claim 1 further comprising invoking an emulation mode of the processor after executing an instruction.

4. The method of claim 1 wherein selecting the debugging mode comprises selecting a first debugging mode when the operating mode comprises user mode, and selecting a second debugging mode when the operating mode comprises supervisor mode.

5. A method comprising:

receiving an instruction;

receiving a signal;

selecting a mode of debugging as a function of the signal, wherein selecting the debugging mode comprises

selecting a first debugging mode when the signal is a first signal, and selecting a second debugging mode when the signal is a second signal; and

executing the instruction.

6. The method of claim 5 further comprising raising an exception.

7. The method of claim 5 further comprising invoking an emulation event.

8. The method of claim 5 further comprising:

sensing register contents; and

outputting register contents.

9. The method of claim 5, wherein the instruction is received by a processor adapted to operate in a plurality of states, the method further comprising:

sensing states of the processor; and

outputting states of the processor.

10. The method of claim 5, wherein the instruction is received by a processor, the method further comprising

selecting a mode of single-step debugging as a function of the operating mode of the processor.

11. A device comprising:

a processor, the processor adapted to operate in a plurality of operating modes including an emulation mode;

a control register adapted to store the state of a control bit; and

an exception handler;

wherein the processor is adapted to select one of a plurality of debugging modes as a function of the control bit.

12. The device of claim 11, wherein the processor is adapted to select one of a plurality of debugging modes as a function of the current operating mode of the processor.

13. The device of claim 11, further comprising exception logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit.

14. The device of claim 11, further comprising emulation logic adapted to sense the state of the control bit and to

trigger an emulation event as a function of the state of the control bit.

15. The device of claim 11, wherein the control bit is a first control bit, the system further comprising a second control bit, and wherein the mode of single-step debugging is a function of the state of the second control bit.

16. The device of claim 11, wherein the processor is a digital signal processor.

17. A device comprising:

a processor, the processor adapted to operate in a plurality of operating modes;

wherein the processor is adapted to select one of a plurality of debugging modes as a function of the current operating mode of the processor.

18. The device of claim 17 further comprising a control register adapted to store the state of a control bit, wherein the processor is adapted to select one of the plurality of debugging modes as a function of the state of the control bit.

19. The device of claim 18, further comprising:

an exception handler; and

logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit.

20. The device of claim 18, further comprising logic adapted to sense the state of the control bit and to trigger an emulation event as a function of the state of the control bit.

21. The device of claim 17, wherein the processor is a digital signal processor.

22. A system comprising:

a processor, the processor adapted to operate in a plurality of operating modes;

a control register adapted to store the state of a control bit;

an input/output device; and

an exception handler;

wherein the processor is to adapted to select one of a plurality of debugging modes as a function of the control bit.

23. The system of claim 22, wherein the processor is adapted to select one of a plurality of debugging modes based upon the current operating mode.

24. The system of claim 22, further comprising a memory device coupled to the processor.

25. The system of claim 22, further comprising logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit.

26. The system of claim 22, further comprising logic adapted to sense the state of the control bit and to trigger an emulation event as a function of the state of the control bit.

27. The system of claim 22, wherein the control bit is a first control bit, the system further comprising a second control bit, wherein the processor is adapted to select one of a plurality of debugging modes based upon the state of the second control bit.